a gate-dielectric layer insulating the first and second floating gates and the portion of the select-gate from the underlying channel region and the first and second junctions,

wherein the cells are serially connected along each row, the select-gates of the cells along each row being connected together forming a plurality of horizontally-extending select-gate lines, the first junction of the cells along each column of cells being connected together forming a first plurality of vertically-extending bitlines, and the second junction of the cells along each column being connected together forming a second plurality of vertically-extending bitlines.

Cont'd B2

REMARKS

Claims 1-18, 21-29, and 37-49 are pending. Claims 1 and 28 are amended to further clarify that the first and second floating gates are non-contiguous. No new matter is believed added. Claims 38-49 have been withdrawn from consideration by the Examiner as being directed to an invention that is independent or distinct from the invention originally claimed. The remaining claims have been rejected as set forth in the following section.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned **"Version with markings to show changes made"**.

35 USC 102(b) and 103(a) rejections:

Claims1-4, 7-9, and 25-26 are rejected under 35 USC 102(b) as being anticipated by Tigelaar USPN 5,273,926. Claims 5, 6, 21-24, 27-29, and 37 are rejected under 35 USC 103(a) as being unpatentable over Tigelaar '926 in view of Guterman '691. Claims 10-18 are rejected under 35 USC 103(a) as being unpatentable over Tigelaar '926. These rejections are respectfully traversed.

The amended claim 1 distinguishes over Tigelaar at least by reciting "first and second non-contiguous floating gates over the channel region".

The Office Action indicates that the first and second floating gates recited in Applicants' claim 1 are shown by floating gate elements 60a, 60b in Fig. 3e of Tigelaar. This is traversed because elements 60a and 60b form part of one floating gate 60, and thus do not constitute "first and second non-contiguous floating gates" as recited in Applicants' claim 1.

Tigelaar in column 5, lines 11-16, in reference to Fig. 5c, states:

> The floating gates 58-62 are shown in phantom, and preferably take the form of hollowed-out rectangles. Portions 100 ... connect the floating gate portions 60a and 60b to be a single conductive unit.

Underline is added. That floating gate portions 60a and 60b form part of a single floating gate is more clearly shown in Fig. 3d. Here, a rectangular portion 82 of floating gate 60 is cut out so that a rectangular opening is created in floating gate 60. Thus, portions 60a and 60b form parts of a single floating gate, not "first and second non-contiguous floating gates" as recited in Applicants' claim 1.

Thus, claim 1 and its dependent claims 2-18 and 21-27 distinguish over Tigelaar at least for the above reason.

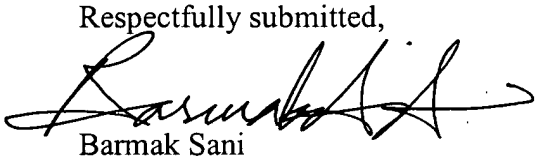
The amended claim 28 includes similar limitations to those discussed above in connection with claim 1, and thus claim 28 and its dependent claims 29 and 37 distinguish over Tigelaar for at least the reasons stated above.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claim 1 has been amended as follows:

1. (Twice Amended) A cell structure comprising:

a first junction and a second junction separated by a channel region, the first and second junctions being in a body region, the separation between the first and second junctions defining a cell channel length extending horizontally, each of the first and second junctions having a vertically-extending width, a horizontally-extending length, and a depth;

first and second non-contiguous floating gates over the channel region; and

a select-gate having a portion between the first and second floating gates, the select-gate also extending over at least a portion of each of the two floating gates and extending across the entire length of each of the first and second junctions, and the select gate being separated from the first and second floating gates only by an insulating layer.

28. (Twice amended) A memory array comprising:

a plurality of cells arranged to form rows and columns of cells, each cell comprising:

a first junction and a second junction separated by a channel region, the first and second junctions being in a body region, the separation between the first and second junctions defining a cell channel length extending horizontally, each of the first and second junctions having a vertically-extending width, a horizontally-extending length, and a depth;

[a] first **[floating gate]** and second non-contiguous floating gates, the first floating gate extending over a first portion of the channel region and over

a portion of the first junction, and the second floating gate extending over a second portion of the channel region and over a portion of the second junction;

a select-gate extending over the two floating gates and extending across the entire length of each of the first and second junctions, the select-gate having a portion between the first and second floating gates, the portion of the select-gate extending over a third portion of the channel region between the first and second channel portions, wherein the first, second, and third portions of the channel region do not overlap and together form the entire channel region;

an inter-polysilicon dielectric layer insulating the first and second floating gates from the select-gate, the select gate being separated from the first and second floating gates only by said inter-polysilicon dielectric layer; and

a gate-dielectric layer insulating the first and second floating gates and the portion of the select-gate from the underlying channel region and the first and second junctions,

wherein the cells are serially connected along each row, the select-gates of the cells along each row being connected together forming a plurality of horizontally-extending select-gate lines, the first junction of the cells along each column of cells being connected together forming a first plurality of vertically-extending bitlines, and the second junction of the cells along each column being connected together forming a second plurality of vertically-extending bitlines.